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[Attached Documents]

[Name of Document] Specification 1
[Name of Document] Drawing 1
[Name of Document] Abstract 1
[Number of General Authorization] 9809938

[Name of Document] Specification

[Title of Invention] Encoding circuit

[Claims]

[Claim 1] An encoding circuit comprising:

a buffer and EOB detector unit for detecting the rearmost non-zero DCT coefficient and outputting the position thereof when DCT coefficients are quantized and are subjected to variable length coding in a zigzag scanning order, and

a variable length coding unit for adding an EOB code to the end of the rearmost non-zero coefficient on the basis of the position from said buffer and EOB detector unit and thereafter pausing the variable length coding process.

[Claim 2] An encoding circuit comprising:

an EOB detector unit for, before DCT coefficients being quantized are subjected to variable length coding, obtaining a correspondence between a zigzag scanning order and the quantized DCT coefficients and detecting a non-zero coefficient having the largest zigzag order among the quantized DCT coefficients, and outputting the largest value, and

a variable length coding unit for adding an EOB code to the end of the non-zero coefficient having the largest zigzag order on the basis of the position from said EOB detector unit and thereafter pausing a variable length coding process.

[Claim 3] An encoder comprising:

an EOB detector unit for obtaining a correspondence between a zigzag scanning order and DCT coefficients prior to quantization before the DCT coefficients are quantized, and detecting a non-zero coefficient having the largest zigzag order on the basis of quantization coefficients, and outputting the largest value, and

a variable length coding unit for adding an EOB code to the end of the non-zero coefficient having the largest zigzag order on the basis of the largest value from said EOB detector unit and thereafter pausing a variable length coding process.

[Claim 4] An encoding circuit comprising:

a rearranging and EOB detection unit for rearranging DCT coefficients prior to quantization in accordance with a zigzag scanning order before the DCT coefficients are quantized, and detecting a non-zero coefficient having the largest zigzag order on the basis of quantization coefficients, and outputting the largest value,

a quantizer for quantizaing the non-zero coefficient having the largest zigzag order on the basis of the largest value from said rearranging and EOB detection unit and thereafter pausing the quantization process, and

a variable length coding unit for adding an EOB code to the end of the rear most non-zero coefficient on the basis of the

position from said rearranging and EOB detection unit and thereafter pausing a variable length coding process.

[Claim 5] A coding method including steps of:

quantizing DCT coefficients;

detecting the position of the rearmost non-zero DCT coefficient in the DCT coefficients or the quantized coefficients; and

pausing a coding process on the quantized DCT coefficients on the basis of the detected position.

[Detailed Description of the Invention]

[0001]

[Technical Field of the Invention]

The present invention relates to an encoding circuit of a digital signal recording/playback apparatus such as a video cassette recorder and a video disk recorder, which digitally records or plays back video or audio signals. More particularly, this invention relates to an encoding circuit of an apparatus that transmits or stores video or audio signals using a variable length coding process.

[0002]

[Prior Art]

To miniaturize a digital signal recording/playback apparatus, it is required to compress enormous amounts of

information of the digital video signals, and record the same.

[0003]

As methods for compressing (encoding) the digital video signals, there are a method employing motion compensation prediction, orthogonal transform, especially Discrete Cosine Transform (DCT), or band division, sampling by quantization, and further a method utilizing Variable Length Coding (VLC) such as Huffman coding, or arithmetic coding. Digital video signals which are compressed by any of the above-mentioned compression methods are transmitted and stored.

[0004]

Among the constructional examples of an encoder, a part of flow after a DCT unit is shown in figure 5. Hereinafter, operation of each block will be described.

[0005]

As shown in figure 5, first, data is inputted to the DCT unit 501. The DCT unit 501 performs a DCT process to the inputted signal, and outputs DCT coefficients to the quantizer 502. The quantizer 502 quantizes the DCT coefficients, and outputs quantized coefficients to the memory 503. The output order of DCT coefficients is shown in figure 6. The memory 503 is a single-port memory including two banks. When the quantized DCT coefficients are stored by one block, the bank is automatically toggled.

[0006]

The encoder 504 carries out zigzag scan on the quantized

DCT coefficients in block units to rearrange the same, and thereafter, carries out two-dimensional variable length coding on the number of preceding coefficients of zero (Run) and a value of a non-zero quantized coefficient (Level) at once. The order of the zigzag scan is shown in figure 7. Further, an EOB (End Of Block) code indicating the end of effective data in that block is added to the end of non-zero coefficient.

[0007]

Meanwhile, the memory 503 may be constituted by a dual-port memory having one bank.

[0008]

[Problems to be solved by the Invention]

In the case of the conventional structure as shown in figure 5, the end of non-zero coefficient cannot be decided until the scanning in the diagonal direction is performed up to the end of this block. Accordingly, the power is consumed wastefully.

[0009]

In view of the above problems, the present invention has for its object to realize an encoding circuit which consumes a reduced power.

[0010]

[Measures for solving the problems]

In order to achieve the above object, the present invention comprises an EOB detector unit for detecting the end of non-zero coefficient and outputting the position thereof as a control

signal and a quantizer or a coding unit which can be paused on the basis of the control signal, wherein the EOB detector unit is provided between a DCT unit and the quantizer or between the quantizer and the coding unit. Accordingly, adaptive consumption power can be reduced without causing a negative influence on the picture quality.

[0011]

[Embodiments of the Invention]

Hereinafter, embodiments of the present invention will be described with reference to the drawings.

[0012]

(first embodiment)

A construction of a coding circuit unit of an encoder according to a first embodiment of the present invention is shown in figure 1. Reference numerals 101-104 in the figure denotes components that are basically similar to those denoted by 501-504 in figure 5 illustrating a conventional construction. Reference numeral 105 denotes a buffer and EOB detector unit.

[0013]

A quantizer 102 quantizes DCT coefficients in a processing sequence shown in figure 6, and stores the quantized coefficients in a memory 103. The memory 103 is a single-port memory including two banks. When the quantized coefficients are stored by one bank, the memory 103 carries out bank switching and outputs the quantized DCT coefficients to the buffer and EOB detector unit 105 in a

processing sequence shown in figure 7.

[0014]

The buffer and EOB detector unit 105 obtains a correspondence between a zigzag order(data processing sequence) and the DCT coefficients as shown in figure 9. When the buffer and EOB detector unit 105 detects the end of non-zero coefficient(non-zero coefficient at which corresponding zigzag order becomes the largest), it outputs the corresponding number of the zigzag order to a coding unit 104 as a control signal 110. Further, after storing the quantized coefficients outputted from the memory 103 in the buffer by one block, the buffer and EOB detector unit 105 outputs the same to the coding unit 104.

[0015]

The coding unit 104 carries out variable length coding on the quantized DCT coefficients outputted from the buffer and EOB detector unit by one block. At that time, when the coding unit 104 detects the end of non-zero coefficient from information of the control signal 110, it adds an EOB signal to the end of non-zero coefficient after the coding, and then, pauses until the last DCT coefficient in the block. The memory 103 can be a dual-port memory including a single bank.

[0016]

(second embodiment)

A construction of a coding circuit unit of an encoder according to a second embodiment of the present invention is shown

in figure 2. Reference numerals 201-204 in the figure denotes components that are basically similar to those denoted by 501-504 in figure 5 illustrating a conventional construction . Reference numeral 205 denotes an EOB detector unit.

[0017]

A quantizer 202 quantizes DCT coefficients in the processing sequence shown in figure 6, and outputs the quantized coefficients to a memory 203 and an EOB detector 205. The memory 203 is a single-port memory including two banks. When the quantized coefficients are stored by one bank, the memory 103 carries out bank switching and outputs the quantized coefficients to a coding unit 204 in the processing sequence shown in figure 7.

[0018]

The EOB detector unit 205 obtains a correspondence between a zigzag order(data processing sequence) and the DCT coefficients as shown in figure 8. When the EOB detector unit 205 detects the end of non-zero coefficient(non-zero coefficient at which the corresponding zigzag order becomes the largest), it outputs the corresponding number of the zigzag order to the coding unit 204 as a control signal 210.

[0019]

The coding unit 204 carries out variable length coding on the quantized DCT coefficients outputted from the memory 203 by one block. At that time, when the coding unit 204 detects the last non-zero coefficient from information of the control signal 210,

it adds an EOB signal to the end of non-zero coefficient after the coding, and then, pauses until the last DCT coefficient in the block.

[0020]

The memory 203 can be a dual-port memory including a single bank.

[0021]

(Third embodiment)

A construction of a coding circuit unit of an encoder according to a third embodiment of the present invention is shown in figure 3. Reference numerals 301-304 in the figure denotes components that are basically similar to those denoted by 501-504 in figure 5 illustrating a conventional construction . Reference numeral 305 denotes an EOB detector unit. A DCT unit 301 outputs DCT coefficients to a quanizer 302 and the EOB detector unit 305 in the processing sequence shown in figure 6.

[0022]

The quantizer 302 quantizes the DCT coefficients in the processing sequence shown in figure 6, and outputs the quantized coefficients to a memory 303. Further, the quantizer 302 outputs quantization coefficients 311 that are used when carrying out quantization to the EOB detecter unit 305.

[0023]

The memory 303 is a single-port memory including two banks. When quantized coefficients are stored by one bank, the memory

303 carries out bank switching and outputs quantized coefficients to an encoder 304 in the processing sequence shown in figure 7.

[0024]

The EOB detector unit 205 obtains a correspondence between a zigzag order(data processing sequence) and the DCT coefficients as shown in figure 8. When the EOB detector unit 305 detects the end of non-zero coefficient(non-zero coefficient at which the corresponding zigzag order becomes the largest), it outputs the corresponding number of the zigzag order to the coding unit 304 as a control signal 310. Since non-zero coefficients have to be decided with an output value of the quantizer 302, they are decided by using the quantization coefficients 311.

[0025]

The coding unit 304 carries out variable length coding on the quantized DCT coefficients outputted from the memory 303 by one block. At that time, when the encoder 304 detects the end of non-zero coefficient from information of the control signal 310, it adds an EOB signal to the last non-zero coefficient after the coding, and then, pauses until the last DCT coefficient in the block.

[0026]

Further, the memory 303 can be a dual-port memory including a single bank.

[0027]

(Fourth embodiment)

A construction of a coding circuit unit of an encoder according to a fourth embodiment of the present invention is shown in figure 4. Reference numerals 401-404 in the figure denotes components that are basically similar to those denoted by 501-504 in figure 5 illustrating a conventional construction. Reference numeral 405 denotes a rearranging and EOB detection unit.

[0028]

A DCT unit 301 outputs DCT coefficients to the rearranging and EOB detection unit 405 in the processing sequence shown in figure 6. The rearranging and EOB detection unit 405 rearranges the inputted DCT coefficients as shown in figure 7.

[0029]

Further, when the rearranging and EOB detection unit 405 obtains a correspondence between a zigzag order and the DCT coefficients and detects the end of non-zero coefficient(non-zero coefficient at which the corresponding zigzag order becomes the largest), it outputs the corresponding number of the zigzag order to the quantizer 402 and the coding unit 404 as a control signal 410. Since non-zero coefficients have to be decided with an output value of the quantizer 402, they are decided by using the quantization coefficients 411.

[0030]

The quantizer 402 quantizes the DCT coefficients in the processing sequence shown in figure 7 and outputs the quantized coefficients to a memory 403. Further, the quantizer 402 outputs

the quantization coefficients 411 that are used when carring out quantization to the rearranging and EOB detection unit 405. Furthermore, when the quantizer 402 detects the end of non-zero coefficient from information of the control signal 410, it pauses until the last DCT coefficeint in the block after quantizing the non-zero coefficient.

[0031]

The memory 403 is a single-port memory including two banks. When the quantized coefficients are stored by one bank, the memory 303 carries out bank switching and outputs the quantized coefficients to a coding unit 404 in the processing sequence shown in figure 7.

[0032]

The coding unit 404 carries out variable length coding on the quantized DCT coefficients outputted from the memory 403 by one block. At that time, when the coding unit 404 detects the end of non-zero coefficient from information of the control signal 410, it adds an EOB signal to the end of non-zero coefficient after the coding, and then, pauses until the last DCT coefficient in the block.

Further, the memory 403 can be a dual-port memory including a single bank.

[0033]

[The effects of the Inventions]

As described above, in the present invention, since an EOB

code insertion position can be identified preliminary, it becomes possible to pause a quantization process or a variable length coding process from the EOB code insersion position to the last DCT coefficient in a block. Accordingly, adaptive consumption power can be reduced without causing a negative influence on the picture quality.

[Brief Description of the drawings]

[Figure 1]

Figure 1 is a block diagram illustrating an encoding circuit according to a first embodiment of the present invention.

[Figure 2]

Figure 2 is a block diagram illustrating an encoding circuit according to a second embodiment of the present invention.

[Figure 3]

Figure 3 is a block diagram illustrating an encoding circuit according to a third embodiment of the present invention.

[Figure 4]

Figure 4 is a block diagram illustrating an encoding circuit according to a fourth embodiment of the present invention.

[Figure 5]

Figure 5 is a block diagram illustrating a conventional encoding circuit.

[Figure 6]

Figure 6 is a diagram illustrating one example of data processing sequence at A shown in figures 1-5.

[Figure 7]

Figure 7 is a diagram illustrating one example of data processing sequence at B shown in figures 1-5.

[Figure 8]

Figure 8 is a diagram illustrating a relationship between the data processing sequence at A in figure 6 and an EOB.

[Figure 9]

Figure 9 is a diagram illustrating a relationship between the data processing sequence at B in figure 7 and an EOB.

[Description of the Reference Numerals]

101...DCT unit

102...quatizer

103...memory

105...buffer and EOB detector unit

201...DCT unit

202...quantizer

203...memory

204...coding unit

205...EOB detector unit

301...DCT unit

302...quantizer

303...memory

304...coding unit

305...EOB detector unit

401...DCT unit

402...quatizer

403...memory

404...coding unit

405...rearranging and EOB detection unit

[Name of The Document] Abstract

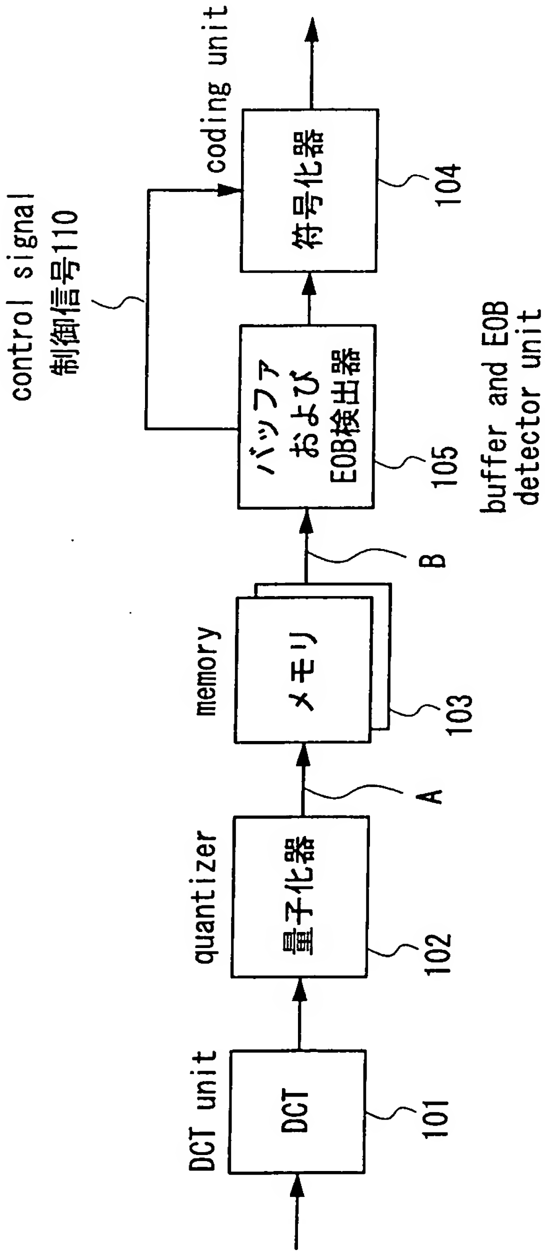
[Summery]

[Object] When subjecting quantized DCT coefficients to variable length coding, a variable length coding unit is controlled while considering a coding process sequence of the DCT coefficients and preliminarily judging the end of significant coefficients so as to achieve low power consumption of the circuit.

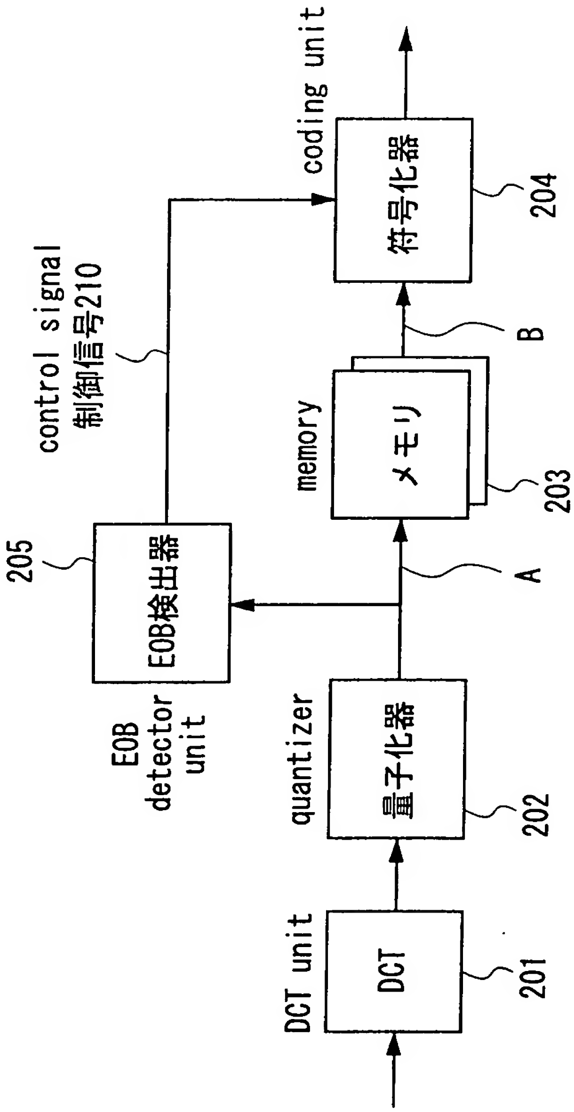
[Solution] The present invention comprises a EOB detector unit 205 for detecting the end of non-zero coefficient and outputting the position thereof as a control signal and a coding unit 204 which can be paused on the basis of the control signal, wherein the EOB detector unit 205 is provided between a quantizer 202 and the coding unit 204. Accordingly, adaptive consumption power can be reduced without causing negative influences on the picture quality.

[Selected Figure] Figure 2

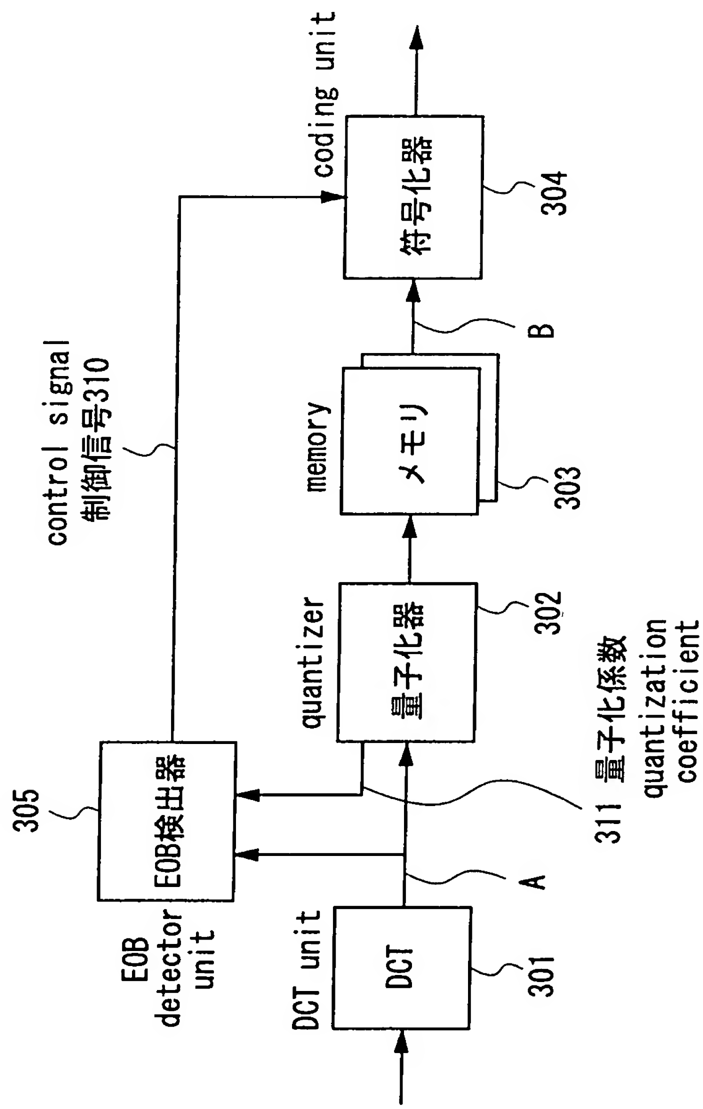
Name of Document
【書類名】　図面 Drawing
【図1】 Figure 1



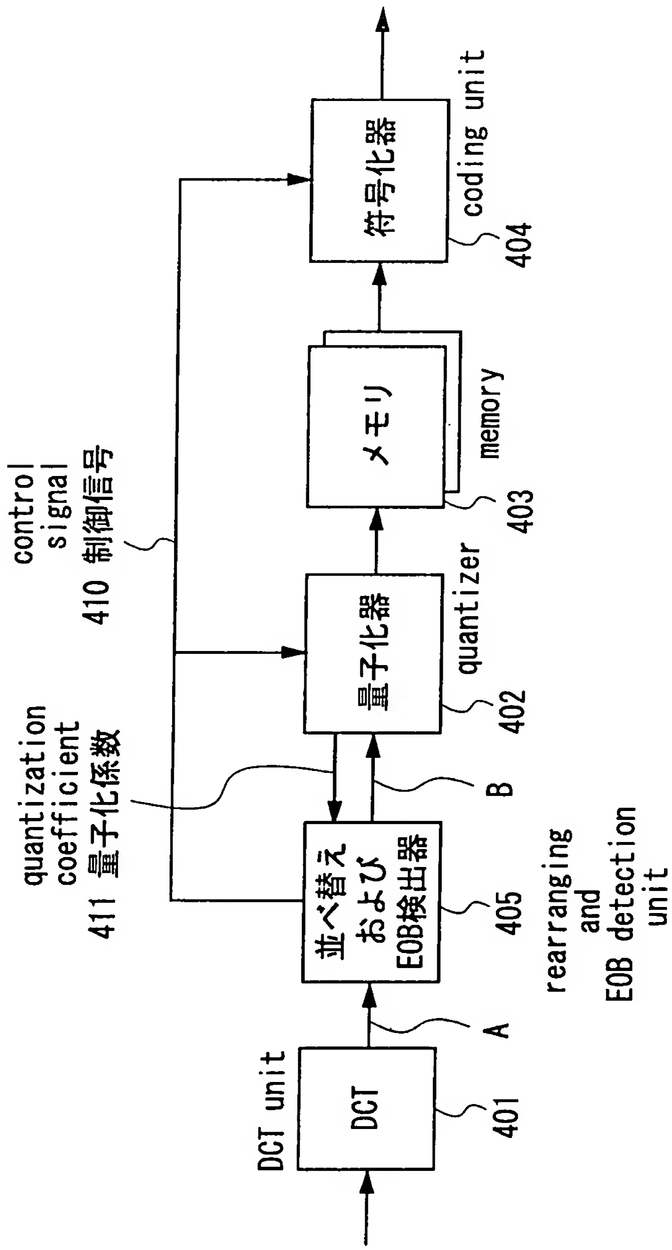
【図2】 Figure 2


DCT unit
DCT
201
quantizer
量子化器
202
A
EOB detector unit
EOB検出器
205
control signal
制御信号210
memory
メモリ
203
B
coding unit
符号化器
204

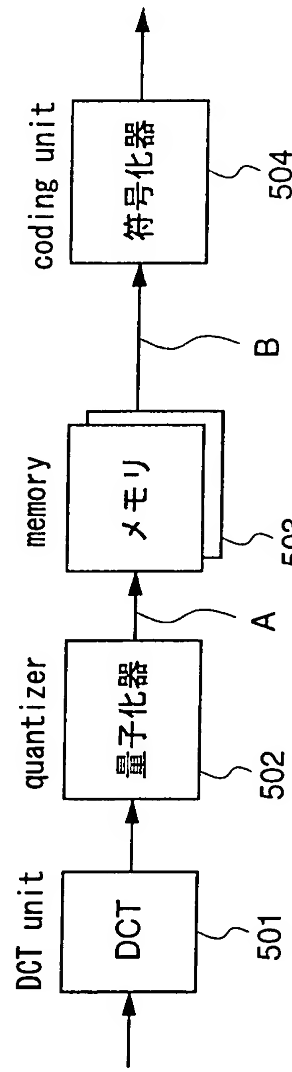
【図3】 Figure 3


coding unit
符号化器
304
B
control signal
制御信号310
memory
メモリ
303
quantizer
量子化器
302
311 量子化係数
quantization
coefficient
305
EOB検出器
EOB
detector
unit
DCT unit
DCT
301
A

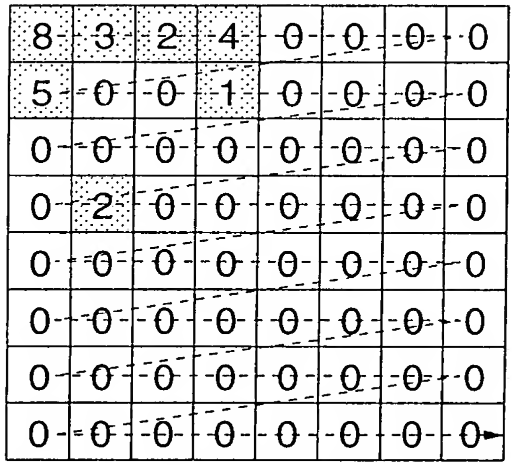
【図4】 Figure 4


DCT unit
DCT
401
A
並べ替え
および
EOB検出器
405
rearranging
and
EOB detection
unit
quantization
coefficient
411 量子化係数
B
量子化器
quantizer
402
control
signal
410 制御信号
メモリ
memory
403
符号化器
coding unit
404

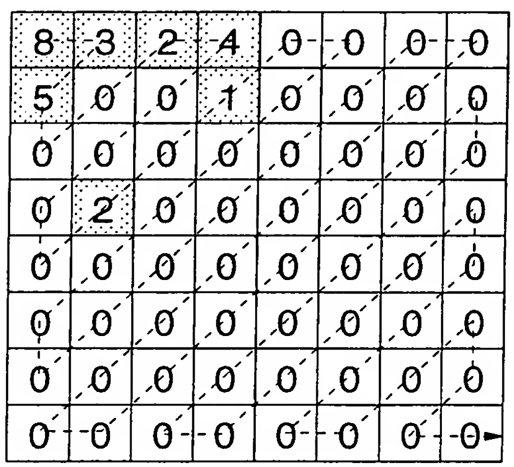
【図5】 Figure 5


DCT unit
DCT
501
quantizer
量子化器
502
A
memory
メモリ
503
B
coding unit
符号化器
504

【図6】 Figure 6



【図7】 Figure 7



【図8】 Figure 8

zigzag order ジグザグ順	1	2	6	7	15	16	28	29	3	5	8	14	17	…	10	12	19	…	64
DCT係数 DCT coefficient	8	3	2	4	0	0	0	0	5	0	0	1	0	…	0	2	0	…	0

EOB

【図9】 Figure 9

zigzag order ジグザグ順	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	…	64
DCT係数 DCT coefficient	8	3	5	0	0	2	4	0	0	0	0	2	0	1	0	…	0
														EOB			